ABSTRACT OF THE DISCLOSURE

The invention provides a method and circuit for measuring on-chip, cycle-to-cycle, jitter. Copies of a circuit comprising a programmable delay line, a programmable phase comparator, and two counters are placed at different locations on an IC near a clock signal. The programmable delay line creates a clock signal that is delayed by one clock cycle. This delayed clock signal is compared in time to the original clock signal by the programmable phase comparator. If the difference in time between the delayed clock signal and the clock signal is greater than the dead time, the first counter is triggered. If the difference in time is negative and the absolute value is greater than the dead time, the second counter is triggered. A statistical distribution, based on the values of the counters, is created. This distribution is used to predict on-chip, cycle-to-cycle jitter.